FET Up-Converter Design Using Load-Dependent Mixing Transconductance

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Abstract — **A new method for a more accurate prediction of FET up-converter gain has been developed. The method uses an equivalent circuit containing a conversion current source at the upper and lower sideband output frequency. The magnitude of the current is related to the IF input voltage by the mixing transconductance factor, which is not a constant but a function of internal LO voltages in the FET. These in turn depend on the output load impedance at the LO frequency. With this approach, we can optimize the output network for acceptable match at the selected sideband and for desired LO signal rejection, while avoiding those impedance values in the LO frequency range that have been observed to cause severe degradation in conversion gain.**

I. Introduction

A GOOD DEAL of research has been conducted on the use of GaAs MESFET's in frequency conversion circuits such as mixers and multipliers. Much of this effort concentrated on determining the dependence of conversion efficiency on gate bias, the optimum input LO power, and, in some cases, the optimum terminating impedances at all ports for the various signal frequencies. This resulted in approximate guidelines for the design of FET mixers. Yet, when these are used in actual practical mixer design, significant deviations from the expected behavior may be observed. This depends on the application (down-converter or up-converter), on mixer type according to how the LO signal is applied to the FET (gate mixer, drain mixer), on the transistor, and on the frequencies involved.

Harrop and Claasen [1] identified the optimal LO drain impedance (i.e., that causing the highest conversion gain) for a gate mixer to be a short circuit. More recently, Maas [2] indirectly justified the choice by stating that a "well-behaved" FET transconductance mixer (i.e., gate mixer) should always operate in the current saturation region and with the lowest LO drain voltage. This implies a short circuit across the drain–source resistance.

For down-converters, where the IF and LO frequencies are usually quite far apart, a short circuit for the LO frequency, placed at the IF port (drain in case of a gate mixer), appears to be a satisfactory and easily realizable approximation of optimum LO loading. In up-converters, the usual proximity of the output and LO frequencies makes it difficult to design the output circuit for an acceptable match at the selected sideband (LO + IF or LO − IF), while maintaining the recommended short-circuit condition in the LO frequency range, particularly if that range is quite wide (e.g. in satellite earth stations). This is true even in balanced configurations. For example, a special tunable combiner at the output was used by the authors of [3] to experimentally overcome the above problem in a balanced FET up-converter.

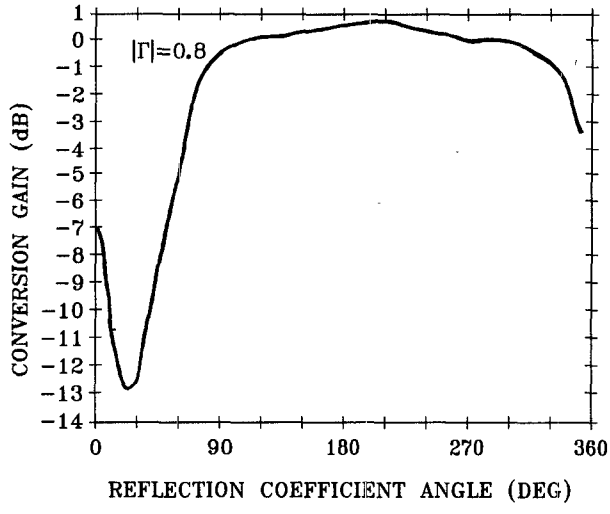

Fig. 1. An example of conversion gain dependence on the reflection coefficient angle of the drain load at the LO frequency

When the LO drain impedance does deviate from the optimum value, a serious impairment to the up-converter performance may occur. In agreement with the results of [3], our measurements with a highly reflective load at the LO frequency showed a significant gain variation over the full 360° range of the reflection coefficient angle of the drain load. A typical example of such conversion-gain behavior is shown in Fig. 1. Note the sharp dip of about 13 dB over a narrow range of values of the reflection coefficient angle. This suggests that avoiding the region of gain minimum rather than maximizing gain should be the goal of an FET mixer design.

It is the aim of this work to contribute to more accurate MESFET up-converter design by thoroughly investigating the LO loading phenomenon and integrating the results into a simulation procedure. The approach described below relies on combining measurements and equivalent circuit representations with commercial frequency-domain

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CAD tools, allowing real-time circuit analysis and synthesis to be made.

The model described in this work will be most useful in cases where the LO range (and therefore the output range) is quite wide. A typical example may be up-converters in ground stations for satellite communication systems, with a 500 MHz bandwidth at a 6 or 14 GHz center frequency. Regardless of the bandwidth, the model should also help in monolithic implementations lacking tuning capabilities.

II. Assumptions and Constraints

Our main objective in this work is to devise a method of simulating the dependence of FET up-converter gain on the drain-circuit impedance at the LO frequency. However, this dependence has to be isolated from other effects known to influence FET mixer conversion gain. Specifically, for a gate up-converter, the following effects will be taken into account:

a) Impedance variations of the gate termination at the output frequency: this will be eliminated by introducing the IF and LO signals to the gate by means of a wide-band, 50 Ω combiner without matching the gate. Thus the impedance the transistor "sees" at the gate is always very close to 50 Ω over the whole frequency range.
b) Drain-circuit impedance at the LO harmonics: we will suppress this effect by reducing the amplitude of the harmonics. If the mixer is made weakly nonlinear by a suitable combination of gate bias and LO power, the harmonics can be kept low while conversion gain is still acceptable. An additional advantage is that less filtering at the up-converter output is required.
c) Output-circuit impedance at the IF frequency: its influence will be eliminated by short-circuiting the drain of the FET for the IF signal. Such a short circuit can be easily realized by a suitable choke or a quarter-wavelength stub that would not significantly affect the LO or output signals.

With these constraints, it is possible to control the up-converter gain in a predictable way by controlling only the output-circuit impedance at the LO frequency and at the selected output sideband frequency.

We will now make the following assumptions:

1) The FET up-converter with the above constraints will be a pure transconductance mixer; i.e., contributions to the conversion mechanism due to nonlinearities other than that of the drain-current versus gate-voltage characteristics are negligible.
2) The observed conversion gain behavior can be attributed to LO-voltage or field variations in parts of the FET structure affecting the nonlinearity of the device. The internal LO voltages are of course related to the drain-load impedance at the LO frequency.
3) It is possible to represent the up-converter by a simple equivalent circuit, similar to that used in [3], that employs current sources at the IF, LO, and the two first sideband frequencies (LO+IF, LO−IF). For convenience, we shall henceforth refer to the latter as RF. The current of the RF sources is proportional, in the usual way, to the gate–source IF voltage. We hypothesize that the proportionality constant (which can be called mixing transconductance) is in fact a function of the LO voltage across one or more suitable elements of the equivalent circuit. If an element or elements with corresponding LO-voltage dependence on the load can be found, the conversion gain behavior can be simulated by means of the above concept of load-dependent mixing transconductance.

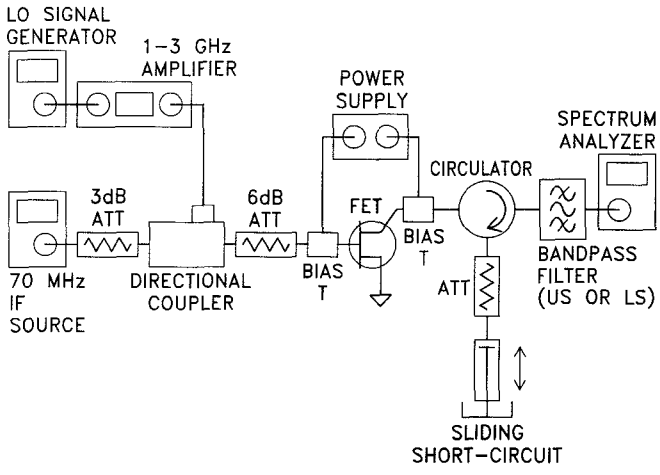

Fig. 2. Conversion gain measurement setup.

The approach proposed here differs in principle from the "classical" work by Curtice *et al.* [4] and others [5]–[7]. There, a specific time-domain function is assigned to the nonlinearity involved and the resulting conversion characteristic is calculated. We will use the measured conversion-gain data to extract the frequency-domain function describing the "mixing transconductance" dependence on the load. It is expected that by using a few carefully selected measurements, the simulation procedure derived in this way will be sufficiently universal to make it possible to simulate the effect of a wide range of loading conditions, originally not covered by the measurements.

III. Conversion Gain Measurements

In order for the proposed method to be valid, the required experimental data must be obtained in a configuration, and under the conditions, that satisfy the above-stated constraints and assumptions.

A suitable experimental setup is shown in Fig. 2. This is a modified load-pull measurement. The bandpass filter is tuned to the selected sideband, thus effectively terminating the transistor by a 50 Ω load for that signal; however, the LO signal is completely reflected and its phase adjusted by the sliding short. The transistor therefore sees a load with a variable reflection-coefficient angle at the LO frequency. The magnitude of the LO reflection coefficient can be

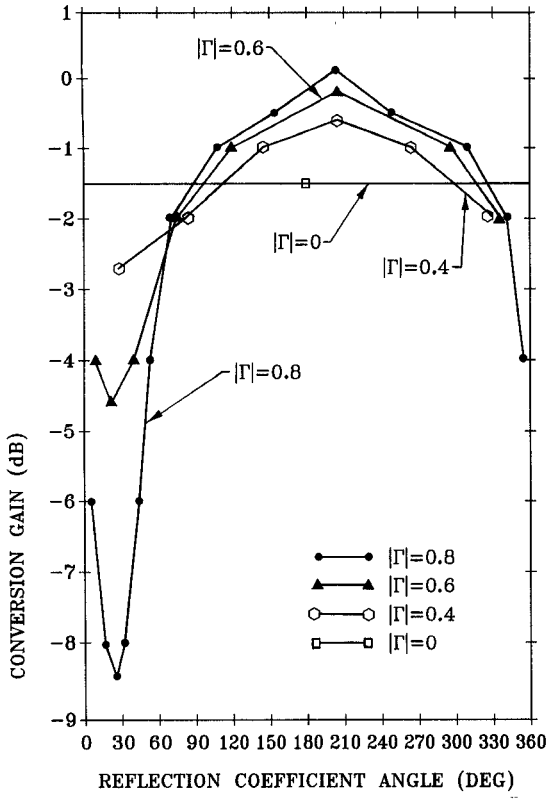

Fig. 3. Measured conversion gain as a function of the drain load reflection coefficient at the LO frequency.

varied by changing the attenuation between the sliding short and the circulator. The maximum of $|\Gamma|$ is limited primarily by the circulator losses (in our case $|\Gamma|_{MAX} = 0.8$). Also, an IF short circuit is added at the drain and no gate matching is used, per c) and a) of Section II, respectively.

Before the FET conversion gain can be measured with this setup, the proper values of gate bias and input LO have to be established. For this, the circulator/filter assembly at the output is temporarily removed and the FET output is directly connected to a spectrum analyzer which represents a broad-band 50 Ω termination. Both the gate bias (V_{gs}^{dc}) and the LO power are now set in such a way that acceptable conversion gain and linearity are obtained while the output level of LO harmonics is kept at least 20 dB below the LO fundamental. This is obviously a subjective adjustment with different results for different intended applications of the up-converter; however, the validity of the method is not compromised as long as the harmonics level is as stated above.

After the operating point has been set, the circulator and filter assembly is replaced and conversion gain measured. At each selected frequency in the LO band, the conversion gain is measured as a function of the sliding short position for a few suitable attenuation values. This yields conversion gain CG as a function of $|\Gamma|$, Θ, and the LO frequency f_{LO}:

$$CG_{MEAS} = CG(|\Gamma|, \Theta, f_{LO}). \tag{1}$$

A typical CG_{MEAS} versus Θ plot, with $|\Gamma|$ as a parameter, is shown in Fig. 3. The particulars (type of FET used, frequency, gate bias, LO power, etc.) are discussed in more detail in Section VI. In general, this plot is similar to that given by Hirota and Ogawa [3]. Note the sharp dip at high $|\Gamma|$ (up to -8.5 dB) and the flat maximum (0 dB), near $\Theta = 180°$. The dip progressively decreases as $|\Gamma|$ does, and the whole curve eventually becomes flat for $|\Gamma| = 0$ (50 Ω load). Clearly, the dip region must be carefully avoided when designing the drain-matching network for an up-converter with this FET.

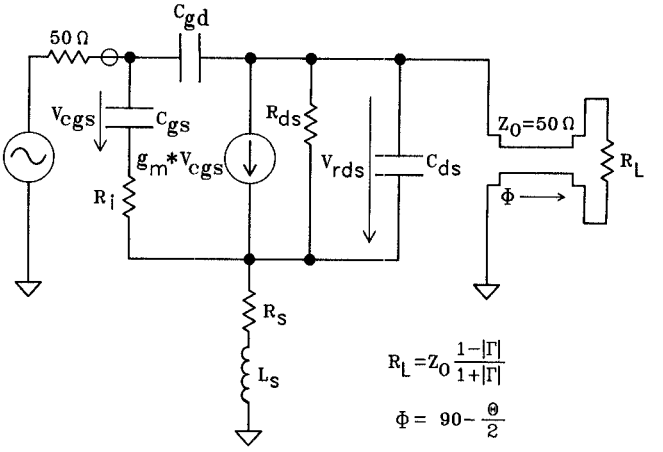

Fig. 4. FET equivalent circuit with variable load.

IV. LO Voltage Patterns in the Equivalent Circuit

Our hypothesis regarding the LO voltage patterns of the FET is tested using an equivalent circuit for the FET valid over the LO frequency range and for the LO level used.

This equivalent circuit, which includes a simple representation of package and chip parasitics, is fitted to the measured S parameters of the FET to extract the values of its elements [8], [9]. The S parameters are measured with the LO level used in the conversion gain measurement. The equivalent circuit is then terminated by a model of the load used in the above conversion gain measurements, and the LO voltage patterns on all elements are examined. The equivalent circuit with the variable impedance load is shown in Fig. 4. By appropriate choice of R_L and Φ, the desired values of the magnitude Γ and angle Θ of the reflection coefficient at the LO frequency can be simulated.

The results of these calculations show that the load dependence of the LO voltages across the gate–source capacitance (V_{cgs}^{LO}) and drain–source resistance (V_{rds}^{LO}) is similar to that of the inverse of the conversion gain. Like conversion gain, the voltages are functions of $|\Gamma|$, Θ, and f_{LO}:

$$V_{cgs}^{LO} = V_{cgs}^{LO}(|\Gamma|, \Theta, f_{LO}) \tag{2a}$$

$$V_{rds}^{LO} = V_{rds}^{LO}(|\Gamma|, \Theta, f_{LO}). \tag{2b}$$

These relations will typically be in the form of graphs of V_{cgs}^{LO} or V_{rds}^{LO} versus Θ with $|\Gamma|$ and f_{LO} as parameters. An example for $|\Gamma| = 0.8$ is shown in Fig. 5(a). Note that the Θ locus of the voltage maxima coincides very closely with

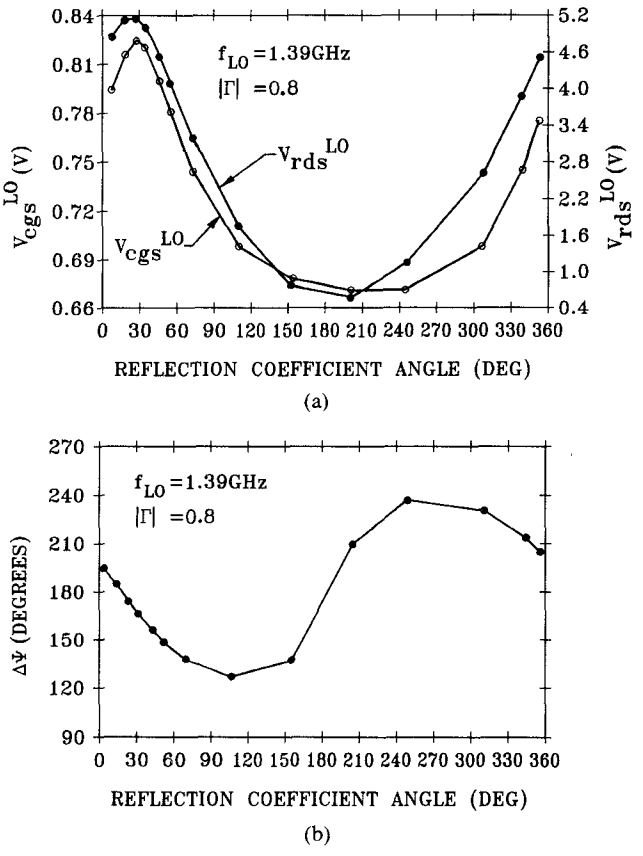

Fig. 5. LO voltages in the FET as a function of the reflection coefficient angle. (a) Magnitude of V_{cgs}^{LO} and V_{rds}^{LO}. (b) Phase difference between V_{cgs}^{LO} and V_{rds}^{LO}.

the minimum conversion gain, and vice versa. The behavior of the phase angle $\Delta\Psi$ between the two voltages is shown in Fig. 5(b). As one would expect, the pattern is centered on an average shift of approximately 180°.

V. Proposed Up-Converter Model

We now present a full FET up-converter model suitable for simulating the demonstrated dependence of conversion gain on the LO loading at the drain. We begin with modifying the FET equivalent circuit by adding current sources at the IF, LO, and the two RF frequencies (upper and lower sideband), as in [3]. The resulting circuit is shown in Fig. 6. The IF and LO sources have the usual transconductance factor associated with it, relating the IF and LO currents to the gate–source voltage at the IF and LO frequency, respectively. The sideband sources have two components: one related to the IF voltage by means of a conversion factor, the mixing transconductance, and the other related to the RF input voltage by "ordinary" transconductance (known from S-parameter measurements). Thus

$$I_{RF} = g_M^{MIX} V_{cgs}^{IF} + g_M V_{cgs}^{RF}. \tag{3}$$

To relate the above expression to the "classical" treatment of FET nonlinearities, we note that the quantities g_M^{MIX} and g_M correspond to the fundamental and dc

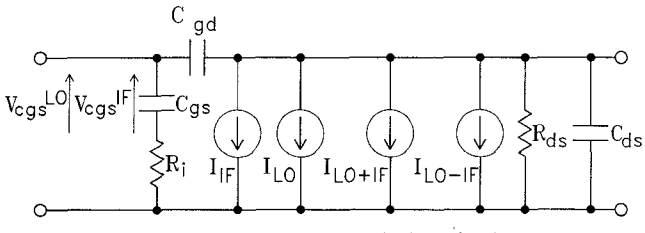

Fig. 6 Up-converter equivalent circuit.

components, respectively, of the time-varying transconductance of the FET, $g_m(t)$.

If we knew g_M^{MIX}, we could now determine the theoretical conversion gain from IF to RF. Since the up-converter is essentially a two-port (LO being an auxiliary signal), this conversion gain is the equivalent of S_{21} in linear two-ports. Its value will be a function of g_M^{MIX}, g_M, and sideband frequency f_{RF}. This S_{21} factor should be equal to the measured conversion gain:

$$S_{21\,CONV}\left(g_M^{MIX}, g_M, f_{RF}\right) = CG_{MEAS}(|\Gamma|, \Theta, f_{LO}) \tag{4}$$

where f_{RF} and f_{LO} are related by f_{IF}. The solution of this equation for g_M^{MIX} yields values of the mixing transconductance for each combination of $|\Gamma|$, Θ, and f_{LO}. We designate this parameter as $g_{M\,MEAS}^{MIX}$ because it is derived from the measured conversion gain data:

$$g_{M\,MEAS}^{MIX} = g_M^{MIX}(|\Gamma|, \Theta, f_{LO}). \tag{5}$$

Equation (5) will be in the form of graphs of $g_{M\,MEAS}^{MIX}$ versus Θ with $|\Gamma|$ and f_{LO} as parameters, rather than an analytical expression.

In accordance with our original hypothesis, we should be able to obtain the mixing transconductance in yet another way. Because of the observed correlation of V_{cgs}^{LO} and V_{rds}^{LO} with the conversion gain, we now postulate that the magnitude of the mixing transconductance is a function of these two voltages. Let us designate g_M^{MIX} obtained in this manner as $g_{M\,CALC}^{MIX}$, since it is derived from the *calculated* voltages, rather than from the *measured* conversion gain:

$$g_{M\,CALC}^{MIX} = g_{M\,CALC}^{MIX}\left(V_{cgs}^{LO}, V_{rds}^{LO}\right). \tag{6}$$

To obtain an explicit form of the above relation, we use the standard technique of multivariable least-square curve fitting for matching a polynomial expression in V_{cgs}^{LO} and V_{rds}^{LO} to the mixing transconductance values obtained in (5). The following expression was found to give the best results for each sample studied:

$$g_{M\,CALC}^{MIX} = \alpha\left(V_{cgs}^{LO}\right)^T + \eta|V_{rds}^{LO}\cos(\Delta\Psi)|^E + \rho|V_{rds}^{LO}\cos(\Delta\Psi)|^G. \tag{7}$$

The phase difference between V_{cgs}^{LO} and $V_{rds}^{LO}(\Delta\Psi)$, shown in Fig. 5(b), is an important variable for a good fit.

The coefficients and exponents of (7) are obtained by a grid search that seeks to minimize an error function that gives an equal effective weight for each data point. The

error function is expressed as follows:

$$\epsilon = \frac{1}{N-m}\sum_{i}^{N}\left\{\frac{g_{M\ \mathrm{CALC}i}^{\mathrm{MIX}} - g_{M\ \mathrm{MEAS}i}^{\mathrm{MIX}}}{g_{M\ \mathrm{MEAS}i}^{\mathrm{MIX}}}\right\}^2 \qquad (8)$$

where N is the number of data points and m is the number of independent variables ($m = 3$ in this case). This is the equivalent of the usual standard error of least-square error regressions.

Expression (7) can now be used to evaluate up-converter performance with any drain load. First, the FET equivalent circuit in Fig. 4 is terminated by the actual drain-matching network, and the two LO voltages, V_{cgs}^{LO} and V_{rds}^{LO}, are calculated. Next the value of the mixing transconductance is determined from (7). Finally, using this value in the FET up-converter equivalent circuit of Fig. 6, the conversion gain can be predicted.

The above would normally be done for a number of frequencies in the range of interest and repeated again for modified parameters of the matching circuit until the best response was obtained. These calculations can be included in an optimization procedure using a CAD program such as Touchstone or Supercompact.

The utility of the method is ultimately determined by the accuracy of $g_{M\ \mathrm{CALC}}^{\mathrm{MIX}}$ obtained in this way over the frequency range of interest. This can be tested by calculating conversion gain for the precise frequencies and values of $|\Gamma|$ and Θ used in the initial conversion gain measurements in the setup of Fig. 2. In contrast to the actual optimization outlined above, these calculations are carried out using 50 Ω as the drain terminating impedance at the desired sideband. This corresponds to the conditions in the measurement setup.

If the conversion gain so calculated closely approximates the measured conversion gain, we can conclude that the optimization procedure described above will be sufficiently accurate for other frequencies in the band and for any drain load exhibiting a reflection coefficient that is within the range used in the measurements. This is discussed in more detail in Section VI.

One of the interesting background aspects of this work is the underlying physical justification for the relationship between the internal LO voltages in the FET and the FET nonlinearity. It appears that internal resonances [10] and the drain-voltage induced shift of the gate pinch-off voltage [7], [11], [12] are responsible for this effect. This shift reduces, in a dynamic way, the nonlinearity of the transconductance. More detail on this and the simulation method as a whole is found in [13].

VI. Simulation Results

The transistors used in this work were low-power, 0.5 μm FET's made by NEC: NE70083 and NE71084. The measurements were carried out over an LO frequency range from 1.39 GHz to 2.03 GHz, with an IF of 70 MHz in each case. The upper sideband was selected. The complete set of measured and calculated data for all the transistor samples used is given in [13]. The following data are typical of the results obtained:

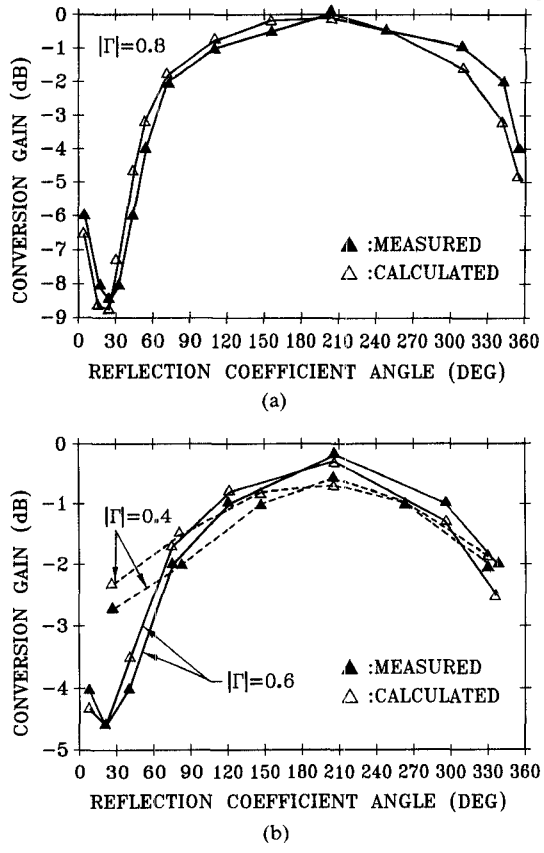

Fig. 7. Comparison of measured and calculated conversion gain at 1.39 GHz: (a) $|\Gamma| = 0.8$; (b) $|\Gamma| = 0.6, 0.4$.

a) LO power of 0 dBm with a typical gate bias of 0.4 V yielded the "optimum" performance with LO harmonics suppressed below −20 dBc.

b) A conversion gain of −2 dB and a third-order intercept point of +6 dBm were measured under the above conditions and with a drain termination of 50 Ω. A maximum of 0 dB gain was obtained for the optimum (short-circuit) drain loading. Note that the value of conversion gain appears low compared to data reported in the literature. However, the latter include the effect of gate matching; no gate matching was attempted here as the focus was on the drain termination problem at the LO frequency. Also, as these measurements used the setup in Fig. 2, the FET drain was not matched at the output frequency either; the filter/circulator assembly, tuned to $f_{\mathrm{RF}} = f_{\mathrm{LO}} + f_{\mathrm{IF}}$, presents a 50 Ω termination to the drain, regardless of the sliding short position at the third port.

c) The average values for the coefficients and exponents in (7) were as follows:

$$T = 0.8 \qquad E = 0.25 \qquad G = 2.5$$
$$\alpha = 0.03 \qquad \eta = 0.01 \qquad \rho = 0.0001.$$

The degree of accuracy obtained with our simulation

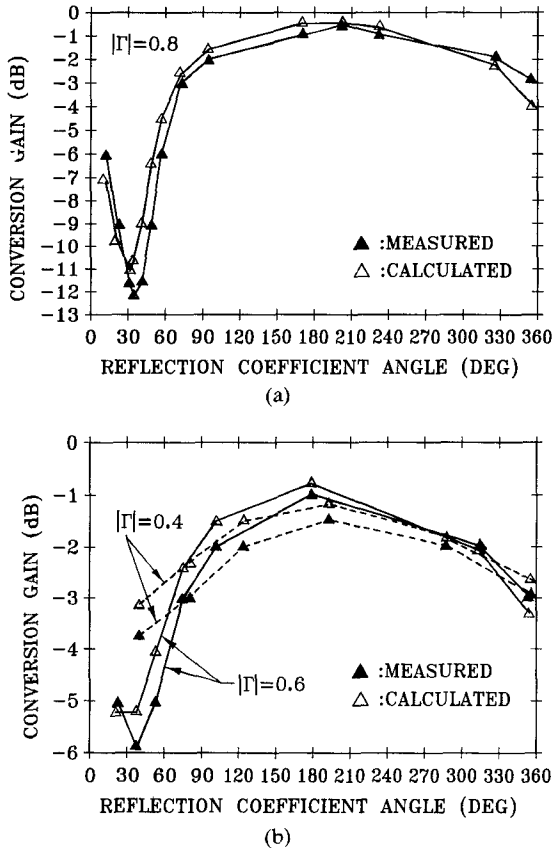

Fig. 8. Comparison of measured and calculated conversion gain at 2.03 GHz: (a) $|\Gamma| = 0.8$; (b) $|\Gamma| = 0.6, 0.4$.

method is best assessed by using graphs of conversion gain versus reflection coefficient angle. The calculated curves are compared to those obtained by measurement in Figs. 7 and 8. In Fig. 7, *CG* versus Θ curves for three different values of $|\Gamma|$ are shown at $f_{LO} = 1.39$ GHz; Fig. 8 shows the same for $f_{LO} = 2.03$ GHz. This is typical of results obtained at other frequencies. The measured and calculated conversion gain curves agree quite closely in shape, but there can be a considerable error for some points within the dip; as much as 3 dB for $|\Gamma| = 0.8$ can be seen in Fig. 8(a) at $\Theta = 45°$. However, given the very steep slope of this notch and the inevitable measurement errors, these deviations are still relatively small. Obviously, the error in measuring Θ_{MIN} at a particular frequency is directly responsible for the magnitude of these deviations.

The reader may suspect that too much measurement effort is required for this kind of simulation. In fact, a very acceptable fit can be obtained from a small amount of data. We found it sufficient to measure the *CG* versus Θ characteristics at the lower band-edge frequency for three values of $|\Gamma|$, and supplement these data by just the extrema points (CG_{MIN}, CG_{MAX}) for a high $|\Gamma|$ (e.g. $|\Gamma| = 0.8$) at a few in-band frequencies. This yielded a good overall match of the calculated and measured conversion gain characteristics for any combination of frequency and $|\Gamma|$. Thus we conclude that the expression for the mixing transconductance obtained in this way, and the element values of the equivalent circuits in Figs. 4 and 6, are accurate enough to be usable for drain load optimization as described in Section V.

VII. Conclusion

The method presented in this paper allows conversion gain simulations of FET up-converters using a few microwave measurements and a simple equivalent circuit. It appears quite suitable as a tool for practical design when used in conjunction with commercially available linear microwave CAD programs.

From a more general point of view, this work has demonstrated the importance of having *some* way of predicting the effect of drain termination impedance in the LO frequency range on the conversion gain of a gate mixer. If the output network were designed solely for matching within the frequency range of the selected sideband, unexpected deep dips in the conversion gain versus frequency characteristics could occur during prototype evaluation, particularly where the LO range is quite wide. The simulation method presented here should prevent such unpleasant surprises from happening.

Acknowledgment

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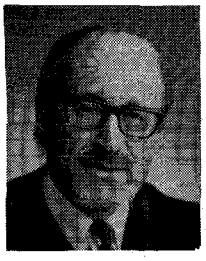

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